UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/987,607	11/15/2001	Hongyong Zhang	740756-2395	7367

31780 7590 04/17/2003

ERIC ROBINSON
PMB 955
21010 SOUTHBANK ST.
POTOMAC FALLS, VA 20165

EXAMINER
HOGANS, DAVID L

ART UNIT	PAPER NUMBER
2813	14

DATE MAILED: 04/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/987,607	ZHANG, HONGYONG	
	Examiner	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-5,7-18 and 20-23* is/are allowed.

6)☒ Claim(s) *1,6,19 and 24-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/585,916* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to Amendment B filed on January 21, 2003.

Status of Claims

Claims 1-23 are pending. Claims 24-28 are newly added.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 6, 24 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by JP362274729 to Katami.

In reference to Claims 1 and 6, Katami teaches:

- forming an interlayer insulator comprising at least upper (106) and lower (105) layers, each comprising different dry etching characteristics (See Figures 1A-1G)

- etching the upper silicon nitride layer (106) using a first mask (107), wherein the lower silicon dioxide layer (105) is used as an etch stopper (See Figures 1A-1G)

- forming a second mask (107) to cover a portion of the silicon dioxide layer, which is exposed by the etching step (See Figures 1A-1G; specifically noting the overlap of photoresist (107) in Figures 1E and 1F)

- selectively etching the lower silicon dioxide layer of the interlayer insulator using the second mask (107) to form a contact hole (See Figures 1A-1G)

In reference to Claims 24 and 25, Katami teaches:

- forming a first interlayer insulating film (105 – silicon dioxide) on a surface (See Figures 1A-1G)

- forming a second interlayer insulating film (106 – silicon nitride) on the first silicon dioxide interlayer insulating film, wherein said silicon nitride insulating film has a different etching characteristic from said silicon dioxide insulating film (See Figures 1A-1G)

- forming an opening in the silicon nitride film by first etching to expose a surface of the silicon dioxide film wherein said silicon dioxide film functions as an etching stopper during the first etching (See Figures 1A-1G)

- forming an opening in the silicon dioxide film by second etching the exposed surface of the silicon dioxide film (See Figures 1A-1G)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 19 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over JP362274729 to Katami. in view of 5,063,378 to Roach.

Claim 19

Incorporating all arguments of Claim 1 and noting that Katami fails to explicitly teach wherein the semiconductor device is a liquid crystal display device.

However, Roach, in columns 5-6 lines 60-20 and Figures 1-3, teaches etching contact vias through a silicon oxide/silicon nitride insulation layer to contact a TFT that is connected to a pixel electrode. Furthermore, Roach teaches that one would do this to provide metallization contacts to the TFT.

It would have been obvious to one of ordinary skill in the art to modify Katami by incorporating the etching of contact vias through a silicon oxide/silicon nitride insulation layer to contact a TFT that is connected to a pixel electrode, as taught by Roach, to provide metallization contacts to the TFT.

Claim 26

Incorporating all arguments of Claim 24 and noting that Katami fails to explicitly teach wherein the semiconductor device is a liquid crystal display device.

However, Roach, in columns 5-6 lines 60-20 and Figures 1-3, teaches etching contact vias through a silicon oxide/silicon nitride insulation layer to contact a TFT that is connected to a pixel electrode. Furthermore, Roach teaches that one would do this to provide metallization contacts to the TFT.

It would have been obvious to one of ordinary skill in the art to modify Katami by incorporating the etching of contact vias through a silicon oxide/silicon nitride insulation layer to contact a TFT that is connected to a pixel electrode, as taught by Roach, to provide metallization contacts to the TFT.

Claim 27

Katami, in Figures 1A-1G, teaches: forming a semiconductor island on an insulating surface; forming a gate insulating film comprising silicon dioxide on the semiconductor island; forming a gate electrode over the semiconductor island with the gate insulating film; forming a first insulating film (105) comprising silicon dioxide over the gate insulating film and the gate electrode; forming a second insulating film (106) comprising silicon nitride on the first silicon dioxide insulating film; first etching the second insulating film to form an opening wherein said silicon dioxide film functions as an etching stopper; second etching a portion of the first insulating film in accordance with the opening of the second insulating film , thereby, exposing a surface of the semiconductor layer.

Katami fails to explicitly teach wherein the gate insulating film is etched.

However, Roach, in Figure 3, shows etching through the extended gate oxide layer. Furthermore, Roach teaches etching through the extended gate oxide layer to create an uninhibited contact to the source/drain region.

It would have been obvious to one of ordinary skill in the art to modify Katami to incorporate etching through the extended gate oxide layer, as taught by Roach, to create an uninhibited contact to the source/drain region.

Claim 28

Incorporating all arguments of Claim 27 and noting that Katami fails to explicitly teach wherein the semiconductor device is a liquid crystal display device.

However, Roach, in columns 5-6 lines 60-20 and Figures 1-3, teaches etching contact vias through a silicon oxide/silicon nitride insulation layer to contact a TFT that is connected to a pixel electrode. Furthermore, Roach teaches that one would do this to provide metallization contacts to the TFT.

It would have been obvious to one of ordinary skill in the art to modify Katami by incorporating the etching of contact vias through a silicon oxide/silicon nitride insulation layer to contact a TFT that is connected to a pixel electrode, as taught by Roach, to provide metallization contacts to the TFT.

5. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over JP362274729 to Katami.

Katami, in Figures 1A-1G, teaches: forming a semiconductor island on an insulating surface; forming a gate insulating film comprising silicon dioxide on the semiconductor island; forming a gate electrode over the semiconductor island with the gate insulating film; forming a first insulating film (105) comprising silicon dioxide over the gate insulating film and the gate electrode; forming a second insulating film (106) comprising silicon nitride on the first silicon dioxide insulating film; first etching the second insulating film to form an opening wherein said silicon dioxide film functions as an etching stopper; second etching a portion of the first insulating film in accordance with the opening of the second insulating film , thereby, exposing a surface of the semiconductor layer.

Katami fails to explicitly teach etching through the gate oxide layer.

However, the specification contains no disclosure of either the critical nature of the claimed methodology or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen methods or upon another variable recited in the claim, the applicant must show that the chosen methods are critical. *In re Woodruff*, 919 F.2d 1575, 1578 (Fed. Cir. 1990)

Allowable Subject Matter

6. Claims 2-5, 7-18 and 20-23 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter.

8. The prior art of record fails to teach Applicant's claimed method for manufacturing a semiconductor device with at least one thin film transistor comprising the steps of: forming a first conductive film; patterning the first conductive film to form a gate electrode; forming an interlayer insulator comprising at least two layers on the gate insulating film; removing a part of an upper layer of the interlayer insulator, the part being located over at least one of a source region and a drain region; forming a contact hole through the interlayer insulator to reach at least one of the source region and the drain region; forming a second conductive film; patterning the second conductive film to form a pixel electrode; forming a third conductive film; and patterning the third conductive film to form at least one of a source electrode and a drain electrode, which is in electrical contact with the pixel electrode.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (703) 305-3361. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (703) 308-4940. The fax phone

numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

dh
April 11, 2003

CARL WHITEHEAD JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800